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ATTORNEYS AT LAW

Docket No.: 247421US2

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

RE: Application Serial No.: 10/752,504
Applicants: Yoshiyuki TANAKA, et al.
Filing Date: January 8, 2004
For: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING OPERATION TEST CIRCUIT AND OPERATION TEST METHOD THEREOF
Group Art Unit: 2138
Examiner: CHUNG, PHUNG M

SIR:

Attached hereto for filing are the following papers:

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE
AMENDMENT UNDER 37 C.F.R. §1.312
LETTER SUBMITTING REPLACEMENT DRAWING SHEET(S)
REPLACEMENT DRAWING 1 SHEET

Our check in the amount of **$0.00** is attached covering any required fees. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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Docket No.: 247421US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION: Yoshiyuki TANAKA, et al.

SERIAL NO.: 10/752,504 GAU: 2138

FILED: January 8, 2004 EXAMINER: CHUNG, P.

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING OPERATION TEST CIRCUIT AND OPERATION TEST METHOD THEREOF

LETTER SUBMITTING REPLACEMENT DRAWING SHEET(S)

COMMISSIONER FOR PATENTS
Alexandria, VA 22313

SIR:

Responsive to the below indicated communication, the following drawing sheets are submitted herewith:

■ 1 Replacement Drawing Sheet ☐ _____ New Drawing Sheets

☐ Official Action dated _____

■ Notice of Allowance/Issue Fee dated June 30, 2006

☐ Other dated _____

The changes and/or modifications made include the following:

Figures 10 and 11 have been amended to replace "PRIOR ART" with the legend "RELATED ART."

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
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DOCKET NO: 247831US2

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF	:
YOSHIYUKI TANAKA, ET AL.	: EXAMINER: CHUNG, P.
SERIAL NO: 10/752,504	:
FILED: JANUARY 8, 2004	: GROUP ART UNIT: 2138
FOR: SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING OPERATION TEST CIRCUIT AND OPERATION TEST METHOD THEREOF	:

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant acknowledges with appreciation the indication of allowability of the claimed invention. In response to the Examiner's Statement of Reason for Allowance in the Notice of Allowance of June 30, 2006, Applicant respectfully submits the following comments.

In the Examiner's Statement of Reasons for Allowance on page 2 of the Notice of Allowance mailed June 30, 2006, paragraph 1 states:

> The following is an examiner's statement of reasons for allowance: Claims 1-20 are allowable over the art of record. This is because the art of record does not disclose or teach the invention as recited in claims 1, 5, 9, 13, 17 and 19, and including a phase control circuit to which a first clock signal is inputted, and which shifts a phase of the first clock signal based on a phase control signal and outputs the resultant signal as a second clock signal;
>
> A first flip-flop to which one of the first clock signal and the second clock signal is inputted as a first operation clock signal, and which operates in synchronization with an edge of

> the inputted first operation clock signal and outputs evaluation data;
>
> A circuit under test to which the evaluation data is inputted and which perform a predetermined process based on the evaluation data and outputs a result of the process as output data; and
>
> A second flip-flop to which the other of the first clock signal and the second clock signal is inputted as a second operation clock signal and the output data is inputted, and which operates in synchronization with an edge of the inputted second operation clock signal and outputs the output data inputted from the circuit under test.

However, although the above statement may be accurate with respect to Claim 1, it is respectfully noted that independent Claims 5, 9, 13, 17 and 19 do not include all of the elements recited above. Accordingly, it is respectfully submitted that the above-quoted statement applies at most to Claims 1-4 and not to any of Claims 5-20.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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